REMARKS

Rejection of claims under 35 U.S.C. §103.

Before proceeding to a point-by-point evaluation of the rejections under 35 U.S.C. §103(a) as to Claims 1-6 and 8-11, Applicant would like to take the opportunity to point out relevant case law which has direct bearing on each of the rejections discussed below. Throughout each of the 35 U.S.C. §103(a) rejections, there exists a commonality with respect to improper combination of references made without proper basis for doing so. As stated in *In re Lee*, 61 USPQ2d 1430 at 1433, "when patentability turns on the question of obviousness, the search for and analysis of the prior art included evidence relevant to the finding of whether there is a teaching, motivation or suggestion to select and combine the references relied on as evidence of obviousness." Here, as was found in *Lee*, Applicant respectfully asserts that disparate references are improperly combined without an adequate basis for doing so because no teaching to combine was provided. Applicant respectfully requests that the improper combination of references based upon circular reasoning not stand, and that the respective claims pass to allowance.

In Sections1-3 of the Office Action, the Examiner rejected under 35 U.S.C. §103(a) Claims 1-6 and 8-11 as being made obvious by Doyle, U.S. patent 5,834,355, in view of Chen et al., U.S. patent 6,489,206. The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited art because a raised source and drain suppresses the short channel effect and acts as an implant mask during halo implant. Applicant respectfully traverses the Examiner's rejection.

The Examiner states that Doyle discloses the steps of:

providing a gate oxide and gate;
performing a source/drain extension implant;
forming a spacer on the gate;
removing the spacer; and
performing a halo implant.

Applicant's reading of the method disclosed by Doyle (col 8, line 51 to col 9, line 66) reveals the following steps:

provide a substrate;
form gate oxide, polysilicon and SiN layers;

pattern SiN layer;
form SiO_2 layer and pattern it;
etch away SiN pattern;
form second SiN layer and pattern it;
form photoresist and pattern it;
etch second SiN pattern and underlying polysilicon;
implant halo ions;
remove photoresist;
remove excess polysilicon to form gate;
remove excess gate oxide;
form source/drain extensions in substrate;
form third SiN layer and pattern it to form gate spacers; and
form source/drain regions in substrate .

Applicant respectfully suggests that the Examiner has inaccurately characterized Doyle by selectively and randomly taking some steps from Doyle and equating them to the claimed sequential steps of Claims 1, 5 and 10. Applicant notes that Claim 1 recites:

A method of making a MOSFET, comprising:
first providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm in length;
second performing a source/drain extension implant;
third forming a spacer on the gate'
fourth performing epitaxy to form raises source/drain regions;
fifth forming a silicide on the gate and source/drain regions;
sixth removing the spacer, thereby forming a void region between the source/drain regions and the gate;
seventh performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and
eighth completing the MOSFET.

While some of the steps of the claimed method can be found in Doyle, Doyle does not teach them in the specific claimed sequence. Additionally, Applicant notes that Doyle teaches the formation of the gate near the end of the sequence, rather than at the beginning. Further, Doyle neither teaches, suggests nor motivates toward formation of a spacer on the gate and its subsequent removal to form a void. Neither does Doyle teach the formation of source/drain extensions in broad contact with the source/drain regions. As shown in Doyle Figure 2S, the extensions (unnumbered) comprise a small area between the source 94/drain 98 regions and the gate 85, with the halo 80 underlying the extensions. The resulting architecture of the

semiconductor thus formed is dissimilar to the architecture of the present invention. Applicant respectfully therefore asserts that Doyle neither teaches, suggests, nor motivates a practitioner to select only a few steps from the lengthy method taught by Doyle and rearrange them into a sequence also neither taught nor suggested. Applicant respectfully maintains that Doyle does not therefore make obvious the presently claimed method.

The Examiner then states that Doyle discloses the claimed invention, except for the limitations disclosed by Chen et al., citing Chen et al. as:

> performing epitaxy to form raised source/drain regions; and
> forming a silicide on the gate and source/drain regions (col 1, lines 15-28).

Applicant's reading of the prior art method disclosed by Chen et al. and cited by the Examiner (col 1, lines 15 to 28), and the subsequent description through line 57, reveals the following steps:

> provide a substrate with isolation regions;
> form gate oxide and gate;
> form source/drain extensions;
> form halo underlying extensions;
> form SiO_2 gate spacers;
> form SiN gate spacers;
> form raised S/D regions; and
> form a silicide over the structure.

Applicant respectfully notes that Chen et al. also teach "However, there are some disadvantages existing in this conventional method. One is the halo implant region 105 surrounding the lightly doped drain region 104 increases the junction capacitance, resulting in a slower operation speed for the MOS device. The other is the misalignment of the ion implant mask can cause changeable LDD/halo implant regions." (col 1, lines 57-63). Thus, while Chen et al. recognize the need to localize the halo around the gate, they fail to teach how to do so in this citation.

Applicant's reading of the method disclosed by Chen et al. (col 2, line 56 to col 3, line 48) reveals the following steps:

> provide substrate with isolation regions;
> form gate oxide and polysilicon gate;
> form SiO_2 gate spacers;

form SiN gate spacers;
form raised source/drain regions;
remove SiN gate spacers to form void;
form source/drain extensions through void; and
form halo through void.

Applicant notes that Chen et al. teach the formation of source/drain extensions only in a narrow area immediately surrounding the gate; these extensions are placed to some depth into the substrate and do not extend appreciably under the raised source/drain regions. Thus, Chen et al. fail to recognize, suggest, or teach any advantage to maintaining the extensive junction between the source/drain extensions and the raised source/drain regions. The implanted halo taught by Chen et al. is implanted in the same manner and space as are the extensions, therefore the halo is essentially equal in area to the source/drain extensions and underlies them in the substrate. The resulting architecture of the semiconductor fabricated by the method taught by Chen et al. is therefore different from that of the semiconductor fabricated according to the method of Claims 1, 5 and 10. Applicant therefore asserts that the method of Chen et al. does not make obvious the method of Claims 1, 5 and 10.

Applicant's Claim 1 recites:

A method of making a MOSFET, comprising:
first providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm in length;
second performing a source/drain extension implant;
third forming a spacer on the gate'
fourth performing epitaxy to form raises source/drain regions;
fifth forming a silicide on the gate and source/drain regions;
sixth removing the spacer, thereby forming a void region between the source/drain regions and the gate;
seventh performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and
eighth completing the MOSFET.

Claims 5 and 10 are similar variants of Claim 1. Applicant respectfully maintains that neither Doyle nor Chen et al., either individually or collectively, teach, suggest, or motivate a practitioner to use the method of Claims 1, 5 or 10, to:

1) form source/drain extensions shallowly in the substrate and extending essentially between the gate and whatever field definition structures are used;

2) form raised source/drain structures completely underlain by lightly doped source/drain extensions;

3) form a silicide over the raised source/drain structures; and

4) form a halo localized around the gate and underlying only a portion of the source/drain extensions.

Finally, in the concluding paragraph of Section 3, the Examiner states "Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wu with Pan, because the raised source and drain suppresses the short channel effect and acts as a implant mask during halo implant, like the photo resist of Doyle." The Examiner neither identifies "Wu" and "Pan", nor explains their significance in relation to the presently claimed method. Wu and Pan have been cited variously in previous Office Actions mailed on March 28, 2002; August 14, 2002; and January 28, 2003; and respectively traversed in Applicant's responses mailed on May 30, 2002; October 31, 2002 and March 28, 2003. Applicant respectfully asserts that the combination of Wu and Pan, in the absence of any further explanation by the Examiner, neither teaches nor suggests the presently claimed invention as discussed in Applicant's responses identified supra. Applicant respectfully maintains that the presently claimed invention, a method citing a specific sequence of steps, thereby achieving improved short channel characteristics of a sub-micron MOSFET, is not made obvious by the cited art, either individually or in combination. Thus, Applicant traverses the Examiner's rejection on this ground and respectfully requests that this rejection be withdrawn and Claims 1-6 and 9-11 be passed to allowance.

In Section 4 of the Office Action, the Examiner stated that the cited art disclosed the claimed invention except for the implant depth of either the source/drain extension or the halo, and that it would have been obvious to one of ordinary skill in the art at the time the invention was made, to implant the dopants at the claimed ranges of depth *since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art* (emphasis added). The Examiner therefore rejected Claims 2, 4, 5, 9 and 10. The Applicant respectfully traverses the Examiner's statement that the cited art has disclosed the general conditions of Claims 1, 5 and 10. Applicant respectfully asserts that the combination of the cited art postulated by the Examiner, in the absence of any suggestion or teaching by Doyle, Chen, Wu or Pan to so

combine, is impermissible under *Lee*, or *In re Zurko*, 59 USPQ2d 1693 (CA FC 2001), and therefore the cited art does not make obvious the claimed method of Claims 1 and 5 to provide the engineered short channel effects in an efficient manner. By eliminating many of the steps taught by Doyle, forming the source/drain extensions completely under the source/drain regions, and localizing the halo around the gate and under only a portion of the extension regions, Applicant has claimed a method not obvious from the cited art. Dependent claims 2, 4, and 9 properly depend from independent Claims 1 and 5 and are therefore allowable for reason of their dependency. Therefore, Applicant respectfully requests reconsideration by the Examiner, withdrawal of this rejection of Claims 2, 4, 5, 9 and 10, and their passage to allowance.

CONCLUSION

Applicant respectfully submits that the presently claimed invention is patentably distinct over the cited references, and Applicant therefore believes that the claims are non-obvious in view of Doyle, Chen et al., Wu and Pan as required by 35 U.S.C. §103 and as published in *Lee* and *Zurko*. Therefore Applicant believes the present invention as now claimed is patentable. In view of the foregoing remarks, favorable consideration by the Examiner, withdrawal of the present rejections, allowance of the pending claims, and passage of the present application to issuance are accordingly solicited. The Examiner is cordially invited to telephone the undersigned for any reason which would advance the pending claims toward allowance.

Respectfully submitted,

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